



AMD-762™ System Controller Revision Guide

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Preliminary Information

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Revision History

Date	Rev	Description
April 2003	G	Added C0 silicon information
October 2002	F	Added errata #56
April 2002	E	Added errata #55
February 2002	D	Added errata #54
May 2001	C	Initial public release

AMD-762™ System Controller Revision Guide

The purpose of the *AMD-762™ System Controller Revision Guide* is to communicate updated product information on the AMD-762™ system controller to designers of computer systems and software developers. This guide consists of four major sections:

- **Product Marking Identification:** This section, which starts on page 5, provides product types, product revisions, OPNs (Ordering Part Numbers), and product marking information.
- **Product Errata:** This section, which starts on page 6, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification. A product errata may cause the behavior of the AMD-762 system controller to deviate from the published specifications.
- **Revision Determination:** This section, which starts on page 16, describes the registers that identify the current revision of the part.
- **Technical and Documentation Support:** This section, which starts on page 17, provides a listing of available technical support resources.

Revision Guide Policy

Occasionally, AMD identifies deviations from or changes to the specification of the AMD-762 system controller. These changes are documented in the *AMD-762 System Controller Revision Guide* as errata. Descriptions are written to assist system and software designers in using the AMD-762 system controller and corrections to AMD's documentation on the AMD-762 system controller are included. This release documents currently characterized product errata.

1 Product Marking Identification

1.1 Production Marking

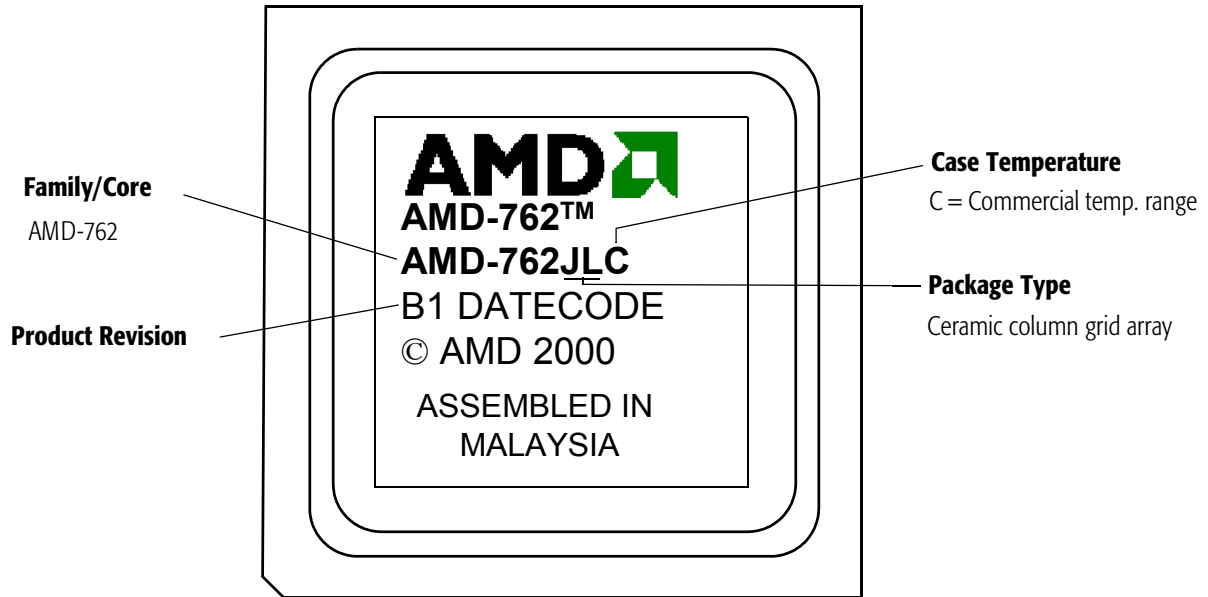


Table 1. Valid Combinations for Ordering Parts

OPN	Package Type	Operating Voltage	Case Temperature
AMD-762JLC	949-pin CCGA	2.375V–2.625V	85°C
Note: Valid combinations are configurations that are or will be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.			

2 Product Errata

This section documents AMD-762 system controller product errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 2 cross-references the revisions of the controller to each erratum. An “X” indicates that the erratum applies to the revision. The absence of an “X” indicates that the erratum does not apply to the revision.

Note: *There can be missing errata numbers. Errata that have been resolved from early revisions of the controller have been deleted, and errata that have been reconsidered may have been deleted or renumbered.*

Table 2. Cross-Reference of Product Revision to Errata

Errata Numbers and Descriptions	Revision ID		
	B0	B1	C0
4 GART Requestors Not Designed to Work with TLB Caches Off	X	X	X
29 External PCI Master to APC Target Resulted in an Extra Null Data Phase	X	X	X
48 AGP Transactions are Non-functional	X		
51 Missed Refreshes When Burst Refresh is Enabled	X		
52 False ACK When Switching from Two-Bit Time to Four-Bit Time Mode	X	X	X
53 AMD-762™ System Controller Enters Connect State Without PROCRDY in C2 Power Management State	X		
54 AGP Compensation Cycle Causes Data Corruption During AGP Writes	X	X	X
55 Heavy PCI/AGP Bus Traffic Can Affect PCI/AGP Ordering	X	X	
56 System Hangs During Prefetches Into 640K-1M Segment	X	X	X

4 GART Requestors Not Designed to Work with TLB Caches Off

Products Affected. B0, B1, C0

Description. Only partial support exists for the mode where GART TLB caches are disabled. GART caches disabled was intended primarily for performance evaluation, and is not supported.

Potential Effect on System. None

Suggested Workaround. The BIOS should set BAR1: Offset 02h bit 2.

Resolution Status. None required, proper operation.

29 External PCI Master to APC Target Resulted in an Extra Null Data Phase

Products Affected. B0, B1, C0

Description. A doubleword write from an external PCI Bus master to external APC target (AGP device) results in an extra null data phase.

Potential Effect on System. No observed effect, except an additional null data phase. This should not be noticeable since it is only a 15 nS data phase, and PCI to APC writes are rare in most systems.

Suggested Workaround. None required, normal operation.

Resolution Status. None.

48 AGP Transactions are Non-functional

Products Affected. B0

Description. AGP cycles are non-functional in this silicon revision due to a silicon development tools issue.

Potential Effect in System. The system may hang when attempting to use AGP cards.

Suggested Workaround. AGP cards can still be used in PCI mode (including PCI mastering) but actual AGP cycles do not. To use AGP cards, do not load the AGP miniport driver in the system. This will force the AGP card to run only PCI cycles.

Resolution Status. Fix planned for a future silicon revision.

51 Missed Refreshes When Burst Refresh is Enabled

Products Affected. B0

Description. The DRAM refresh period may be violated in some cases when the burst refresh feature is enabled in the DRAM Mode/Status Register. The burst refresh feature allows multiple refresh requests to be queued up before holding off any memory requests, but the AMD-762 system controller may violate the maximum refresh rate under very heavy loading conditions. This occurs only when burst refresh is enabled.

Potential Effect on System. Data corruption or hard locks when running with burst refresh enabled. This has been observed only in very harsh memory testing, and has never been observed when running any Microsoft® Windows® operating systems.

Suggested Workaround. Disable the burst refresh feature by writing a zero to bit 20 of the DRAM Mode/Status Register (Dev 0:F0:0x58).

Resolution Status. Fix planned for a future silicon revision.

52 False ACK When Switching from Two-Bit Time to Four-Bit Time Mode

Products Affected. B0, B1, C0

Description. The P0_2BitPF bit and P1_2BitPF bit (Two Bit Times Per Frame Enable) in the Extended BIU Control Register are specified to be set when running with an AMD Athlon™ processor, or cleared when running with an Alpha™ processor. Setting these bits (enabling 2-bit times per frame), and subsequently clearing the bits, can cause the AMD-762 system controller to return a false ACK to the processor, resulting in system failures.

Under normal conditions these bits should not be changed once it is initialized by the system BIOS. Changing the value of the bits from a zero to a one is considered normal operation and does not cause the failure.

Potential Effect on System. System may hard lock when changing either the P0_2BitPF bit or the P1_2BitPF bit in the Extended BIU Control Register from one to zero.

Suggested Workaround. Do not change either of the “Two Bit Times Per Frame Enable” bits (P0_2BitPF, bit 3, or P1_2BitPF bit 4 of Dev 0:F0:0x44) from a one to a zero. BIOS should set these bits only when running with an AMD Athlon processor, and then not change the value. These bits should be left cleared when running with an Alpha processor.

Resolution Status. None required.

53 AMD-762™ System Controller Enters Connect State Without PROCRDY in C2 Power Management State

Products Affected. B0

Description. When exiting the C2 ACPI power management state, it is possible for the AMD-762 system controller to enter the Connect state when one processor has not actually asserted its PROCRDY signal. The following sequence illustrates the failing case. This sequence follows a probe initiated by an external PCI bus master read, with two processors installed in the system.

- The AMD-762 system controller deasserts CONNECT to P1, followed shortly by deasserting CONNECT to P0. Note that STPCLK# has been deasserted by the Southbridge at this time.
- Processor 1 responds to CONNECT deassertion by slowing its internal clocks, but processor P0 detects that STPCLK# is deasserted before its CONNECT pin is deasserted and continues to assert its PROCRDY pin. This causes the AMD-762 system controller to assert CONNECT to both processors.
- P1 will now lock-up and will not reconnect.

Potential Effect in System. The failure condition will cause the P1 processor to lock up and never reconnect.

Suggested Workaround. When both processors are installed, BIOS should not report C2 capability in the ACPI table and thermal throttling must be disabled.

Resolution Status. Fix planned for a future silicon revision.

54 AGP Compensation Cycle Causes Data Corruption During AGP Writes

Products Affected. B0, B1, C0

Description. A bug in the AGP compensation logic can cause the AMD-762 system controller to drive the AGP data bus while the AGP card has been granted the bus by the AGP arbiter. This occurs only during AGP write cycles and can result in data corruption on the AGP data bus.

Potential Effect on System. Data written to main memory by the AGP card can be corrupted when AGP compensation is enabled in the AMD-762 system controller. The AGP compensation circuitry is only enabled when configured for 1.5V signaling.

Suggested Workaround. The suggested workaround for cards that use 1.5V signaling is to configure the card's AGP driver to not allow the AGP card to perform AGP writes.

Resolution Status. No fix planned.

55 Heavy PCI/AGP Bus Traffic Can Affect PCI/AGP Ordering

Products Affected. B0, B1

Description. Lengthy sequences of memory mapped I/O cycles from a processor to either PCI or AGP that occur during periods of high bus traffic resulting in high bus latency may cause a subsequent sequence of memory mapped I/O operations to the PCI and/or AGP buses that are strongly ordered with respect to the two processors to be performed in a different order.

Potential Effect on System. PCI or AGP memory operations that are strongly ordered between two processors may be seen on the PCI or AGP bus in a different order than intended by software, which may cause failures with certain add-in cards.

This failure can only occur in systems with both processors installed and running and has only been identified by AMD in conjunction with diagnostics.

Suggested Workaround. None.

Resolution Status. Fix planned for a future silicon revision.

56 System Hangs During Prefetches Into 640K-1M Segment

Products Affected. B0, B1, C0

Description. A system hang occurs when a PCI bus master prefetches into the 640K-1M region while Dev 0:F0:0x84, bit 4 (EV6_Mode) is set and VGA is enabled (Dev 1:F0:0x3C, bit 19). The AMD-762 system controller will forward writes to this region to the AGP card but reads are incorrectly terminated (accepted via DEVSEL# assertion but not forwarded to AGP or DRAM).

Potential Effect on System. System hangs when a PCI bus master prefetches into the 640K-1M region.

Suggested Workaround. BIOS should reserve the area directly below A0000h to prevent prefetching into the 640K-1M region.

Resolution Status. No fix planned.

3 Revision Determination

Table 3 summarizes the AMD-762 system controller configuration register offsets, devices, default values after reset, and access types. Access types are indicated as follows:

RW - Read/Write
 RO - Read Only

Table 3. Function 0, Device 0 Configuration Registers

Offset	Field Name	Reset	Access
01h–00h	Vendor ID (AMD)	1022h	RO
03h–02h	Device ID Dual Processor Device	700Ch	RO
08h	Revision ID	nn *	RO
Note: * nn changes for each device revision. For example, 00h = Revision A0; 01h = Revision A1; 10h = Revision B0; 21h = Revision C1; 25h = Revision C5 etc.			

Vendor ID Device 0 Offset 01h–00h

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
Vendor ID															
Reset	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0

This read-only value is defined as 1022h.

Device ID Device 0 Offset 03h–02h

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
Device ID															
Reset	0	1	1	1	0	0	0	0	0	0	0	1	1	0	0

This read-only value of 700Ch represents the AMD-762 system controller dual processor device.

Revision ID Device 0 Offset 08h

Bit 7	6	5	4	3	2	1	Bit 0
AMD-762™ System Controller Chip Revision and Stepping Code							

Reset — — — — — — —

Bits 7–0

AMD-762™ System Controller Revision Code (RO) - The most-significant nibble indicates the die revision and the least-significant nibble represents the stepping. (For example, 00h = Revision A0; 01h = Revision A1; 10h = Revision B0; 21h = Revision C1; 25h = Revision C5; etc.)

4 Technical and Documentation Support

The following documents provide additional information regarding the operation of the AMD-762 system controller:

- *AMD-762™ System Controller Data Sheet*, order# 24416
- *AMD-762™ System Controller BIOS Software/BIOS Design Guide*, order# 24462
- *AMD-766™ Peripheral Bus Controller Data Sheet*, order# 23167
- *AMD Athlon™ System Bus Specification*, order# 21902
- *AMD Athlon™ Processor BIOS, Software, and Debug Tools Developers Guide*, order# 21656
- *AMD Athlon™ Processor Data Sheet*, order# 21016

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